Patent Claims:

1. A process for digital communication between

* a first unit (DSP1), which has at least one input (ESD) for serial digital data,
* at least two second units (3a,3b) with a data output (ASD) for serial, digital data,

whereby the input (ESD) of the first unit (DSP1) is connected via a common data line (SD) to the outputs (ASD) of the second units (3a, 3b) connected to it, and in the process, serial, digital data are supplied from the second units (3a, 3b) to the first (DSP1) over the data line (SD) mentioned, controlled by a binary permission signal fed to the second units (3a, 3b), connected together over a permission line (WS), and a clock signal fed together to the units connected via a clock line (SCL), characterized by the fact that the first unit (DSP1) communicates with the second (3a, 3b) over the permission line (WS), by superimposing data signals (DA) on the binary permission signal on the first unit (DSP1) and by receiving and evaluating them on the second unit (3a, 3b).

2. In a process for digital communication between

* a first unit (DSP1), which has at least one input (ESD) for serial digital data,
* at least two second units (3a,3b) with a data output (ASD) for serial, digital data,

whereby the input (ESD) of the first unit (DSP1) is connected via a common data line (SD) to the outputs (ASD) of the second units (3a, 3b) connected to it, and in the process, serial, digital data are supplied from the second units (3a, 3b) to the first (DSP1) over the data line (SD) mentioned, controlled by a binary permission signal fed to the second units (3a, 3b), connected together over a permission line (WS), and a clock signal fed together to the units connected via a clock line (SCL); a process for identifying how many second

units (3a, 3b) are connected to the first (DSP1), characterized by the fact that serial, digital random signals, each independent of the other, are placed on the common data line (SD) at the second units (3a, 3b) connected, and the signal on the data line (SD) detects whether a predetermined signal state occurs, which clearly expresses the number of second units actually connected.

3. The process in Claim 1, further comprising a process for identifying how many second units (3a, 3b) are connected to the first (DSP1), characterized by the fact that serial, digital random signals, each independent of the other, are placed on the common data line (SD) at the second units (3a, 3b) connected, and the signal on the data line (SD) detects whether a predetermined signal state occurs, which clearly expresses the number of second units actually connected.

4. The process in one of Claims 1 to 3, characterized by the fact that the first unit (DSP1) is a digital signal-processing unit of a hearing aid, and the second units (3a – 3x) are the peripheral units of a hearing aid, like especially acoustic/electric converters, electric actuators, T coils, controls like potentiometers or switches, interface units.

5. The process in Claim 4, characterized by the fact that the peripheral units of the hearing aid work on the data line (SD) via an A/D converter (14).

6. The process in one of Claims 1 or 2, characterized by the fact that random signals are produced by sending a noise signal (18) to an A/C converter (14) working on the data outputs (ASD) on the input side. or, and preferably, using A/D converter – LSB – output signals as noise signals.

7. The process in Claim 2, characterized by the fact that the predetermined signal state is simultaneously only detectable on one of the second units connected.

8. The process in Claim 7, characterized by the fact that on the second unit (3a, 3b) that first detects the given state mentioned, the permission phase (I, II) detected by the permission signal (S_{WS}) on the permission line (WS) is inverted.

9. The process in Claim 2, characterized by the fact that the signal on the data line (SD) on each second unit connected (3a, 3b) is logically interconnected with the signal of the signal placed on that unit by means of a random generator on the data line.

10. The process in Claim 2, characterized by the fact that the random signals of the second units (3a, 3b, 3x) connected are placed on the data line via a "wired AND" interconnection.

11. The process in one of Claims 7 to 10, characterized by the fact that when during a predetermined time span, a second unit (3a, 3b, 3x) that is turned on has not detected the predetermined signal state and no random signal on the data line (SD) is detected on that unit in permission-blocked phases (II) of the permission signal (S_{WS}), the second unit concludes that it is the only one connected to the data line (SD).

12. The process in Claim 11, characterized by the fact that a second unit connected, which identifies itself as the only one connected to the data line (SD), during permission-blocked phases (II) of the permission signal (S_{WS}), switches a defined electric potential on the data line, preferably corresponding to the logic state '0.'

13. The process in Claim 2, characterized by the fact that the identification process is triggered by turning on the electric power to the units.

14. The process in one of Claims 1 to 2, characterized by the fact that more than two second units (3x) can be connected to a first unit (DSP1') and by the fact that for each initiated pair of other second units (3x) another data line (SDx) to another input (ESDx)

of the first unit (DSP1') is provided and for all second units together, a clock line (SCL) and a permission line (WS) are used.

15. The process in one of Claims 1 to 2, characterized by the fact that on at least some of the connected second units, addresses (A) are produced by means of digital random signals.

16. The process in Claim 15, characterized by the fact that the addresses (A) produced are read in on the first unit (DSP1') and then all second units are controlled by the first unit (DSP1') over the permission line (WS), to produce new addresses (A) by means of the random signals, when the addresses read in are identical.

17. The process in one of Claims 1 or 3, characterized by the fact that the data signals superimposed by the first unit (DSP1, DSP1') are produced within a predetermined section of the phase of the permission signal (S_{WS}) on it (S_{WS}).

18. A digitally communicating system, including:

* a first digital processing unit (DSP1), which has at least one input (ESD) for serial digital data,

* at least two second units that can be connected to one data output (ASD) for serial digital data

whereby the input (ESD) of the first unit (DSP1, DSP1') is connected over a common data line (SD) to the outputs (ASD) of the second units (3a, 3b) connected, and the first unit (DSP1, DSP1') is connected by means of a common permission line (WS) to the second units (3a, 3b) connected, whereby the first unit produces a binary permission signal (S_{WS}) on this permission line, and the second units connected controlled by the permission signal, time-staggered for writing data on the common data line (SD) are

controlled and released, whereby the units are connected by means of a common clock line (SCL), characterized by the fact that a coding unit (ENC) is provided on the first unit (DSP1) to superimpose data signals on the permission signal (S_{WS}) on the permission line (WS) and by the fact that a decoding unit (DEC) is connected to the input of the permission line (WS) on each second unit connected (3a,3b, 3x), in order to decode data signals (DA) superimposed on the permission signal (S_{WS}) in addition to data write permission (SW).

19. A digitally communicating system, including:

* a first digital processing unit (DSP1), which has at least one input (ESD) for serial digital data,

* at least two second units that can be connected to one data output (ASD) for serial digital data

whereby the input (ESD) of the first unit (DSP1, DSP1') is connected over a common data line (SD) to the outputs (ASD) of the second units (3a, 3b) connected, and the first unit (DSP1, DSP1') is connected by means of a common permission line (WS) to the second units (3a, 3b) connected, whereby the first unit produces a binary permission signal (S_{WS}) on this permission line, and the second units connected controlled by the permission signal, time-staggered for writing data on the common data line (SD) are controlled and released, whereby the units are connected by means of a common clock line (SCL) characterized by the fact that a digital random generator (14, 18) can be connected to work with the data line (SD) on each second unit connected and controlled (3a, 3b, 3x), and a comparison unit (22) is also provided, which is connected to work with the data line (SD) and the random generator output.

20. The system in Claim 18, further characterized by the fact that a digital random generator (14, 18) can be connected to work with the data line (SD) on each second unit

connected and controlled (3a, 3b, 3x), and a comparison unit (22) is also provided, which is connected to work with the data line (SD) and the random generator output.

21. A hearing aid with the system in one of Claims 18 to 20, characterized by the fact that the first unit is a digital signal-processing unit of the hearing aid, and the second units are peripheral units assigned to the processing unit, like especially acoustic/electric converters, electric actuators, T coils, controls, such as potentiometers or switches, etc.

22. The hearing aid in Claim 21, characterized by the fact that each second unit (3a, 3b,3x) has an A/D converter (14) which is connected to work with the output (ASF) for the data line (SD).

23. The system in one of Claims 19 to 20, characterized by the fact that the random generator has an A/D converter (14).

24. The system in one of Claims 19 to 20, characterized by the fact that the output of the comparison unit (22) inverts the working connection of an input for the permission line (WS) on a write unit (14), which is connected to work with the output (ASD) for the data line (SD), in terms of the binary signal on the input mentioned (24).

25. The system in one of Claims 19 to 20, characterized by the fact that the output (A_{14}) of the random generators (14) of the second units (3a, 3b) connected to the data line (SD) are connected to work with that line (SD) over a "wired AND" interconnection.

26. The system in one of Claims 19 to 20, characterized by the fact that each second unit connected (3a, 3b) has a controllable switching arrangement (36), which is connected to the output (ASD) for the data line (SD) and lays it, controlled by the permission signal on the permission line (WS), on a defined electric potential.

27. The system in one of Claims 19 to 20, characterized by the fact that random generators (14) provided on the second units connected are set in operation by turning on the supply voltage to the second units.

28. The system in one of Claims 18 to 20, characterized by the fact that more than two second units (3x) can be connected to one and the same first unit (DSP1'), whereby the clock line (SCL) and the permission line (WS) run from the first unit (DSP1') together to all peripheral units connected, and a single data line (SDx) runs to the first unit (DSP1') per pair and/or initiated pair of second units (3x) connected.

29. The system in one of Claims 18 to 20, characterized by the fact that a random generator (14) can be connected to each second unit with the data line output (ASD), and they can be triggered by a predetermined sequence of signals on the permission line, whereby a sequence of random signals placed on the data line (SD) on the respective peripheral unit is stored in one memory (40) each, the name sequence on the first unit (DSP1').

30. The system in Claim 29, characterized by the fact that the sequence and – in terms of the permission signal on the permission line (WS) – the write-permission phase are stored as addresses on the second unit and on the first unit in the respective address memory arrangements, and the address memory arrangement on the first unit (DSP1') is connected to a comparison unit, which triggers another sequence of signals on the permission line to second units with identical addresses.

31. The system in one of Claims 18 or 20, characterized by the fact that the coding unit (ENC) on the first unit (DSP1, DSP1') is connected to a time-control unit, which allows superimposed signals (DA) to be given to the permission line (WS) only at predetermined intervals of time in the permission signal cycle.

32. The process in one of Claims 1 or 2, characterized by the fact that random signals are produced using A/D converter LSB output signals as noise signals.